

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Electronic Version v11

Stylesheet Version v10

Title of Invention	JITTER-RESISTIVE DELAY LOCK LOOP CIRCUIT FOR LOCKING DELAYED CLOCK AND METHOD THEREOF				
<p>As the below named inventor, I declare that:</p> <p>This declaration is directed to the invention titled: " JITTER-RESISTIVE DELAY LOCK LOOP CIRCUIT FOR LOCKING DELAYED CLOCK AND METHOD THEREOF"</p> <p>I believe that I am the original and first inventor of the subject matter which is claimed and for which a patent is sought;</p> <p>I have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;</p> <p>I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.</p> <p>All statements made herein of my knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.</p>					
<p>FULL NAME OF INVENTOR:</p> <table border="1" style="width: 100%; border-collapse: collapse;"><tr><td style="width: 50%; padding: 5px;">Inventor: Jui-Hsing Tseng</td><td style="width: 50%; padding: 5px;">Inventor</td></tr><tr><td style="width: 50%; padding: 5px;">Signature :</td><td style="width: 50%; padding: 5px;">Citizen of : TW</td></tr></table>		Inventor: Jui-Hsing Tseng	Inventor	Signature :	Citizen of : TW
Inventor: Jui-Hsing Tseng	Inventor				
Signature :	Citizen of : TW				

PATENT
Docket No MTKP0186USA

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor , I hereby declare that :

I believe I am the sole (if only one name appears below) , or joint (if more than one name appears) , original and first inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled :

**"JITTER-RESISTIVE DELAY LOCK LOOP CIRCUIT FOR LOCKING
DELAYED CLOCK AND METHOD THEREOF"**

+ The specification for the above entitled invention is filed herewith.
The specification for the above entitled invention was filed previously
with application serial number: Filing Date:

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of the invention disclosed in this application in accordance with Title 37, Code of Federal Regulations, Section 1.56 (a). I further acknowledge the duty in any continuation-in-part application to disclose to the Patent and Trademark Office all information known to be material to the patentability of the invention disclosed in this application, as defined in 1.56, which became available to me between the filing date of the prior application and the filing date of this application.

PRIORITY CLAIM

+ There is no claim of priority
Claim of priority is based on the following:

POWER OF ATTORNEY

As a named inventor, I hereby appoint the following attorneys to prosecute this application and to transact all related business in the Patent and Trademark Office:

Winston Hsu Registration# 41,526

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DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued hereon.

(請發明人務必簽署日期)

Date:	08/18/04'	Jui-Hsing Tseng
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and Residence		
Citizen of:		R.O.C.